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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,739	10/30/2003	Yueh-Chuan Lee	0941-0860P	6178

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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,739	LEE ET AL.	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 24-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-23 and 35-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The previous Office Action has been withdrawn according to new search.

Election/Restriction

Applicant's election **with traverse** of claims **16-23 and 35-42** is acknowledged.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims.

The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method' and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL.**

Claim Rejections

Set of claims 16- 23

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16- 23 are rejected under 35 USC 102 (b) as being anticipated by Chen et al. (6239011).

Chen et al. teaches a semiconductor structure with a partially etched gate, comprising:

a semiconductor substrate 10; a gate dielectric layer 16, a gate conductive layer 18/20 and a cap layer 22, sequentially stacked on the substrate to form a gate structure (fig. 3); and a lining layer (thin pad oxide layer, see col 5, lines 25-30) disposed on sidewalls of the gate structure, wherein the lining layer or thin pad oxide layer disposed on one sidewall of the gate structure is partially etched to expose the adjacent gate structure 34 ((col 2, line 30 and fig. 3).

Regarding claim 17, an inter-layer dielectric layer covering the gate structure (fig. 5F); and a bitline contact 42 formed in the inter-layer dielectric layer 28, exposing the substrate 10 and a portion of the gate structure therein, wherein the lining layer 27 of the exposed portion of the gate structure is partially removed.

Regarding claim 18, wherein the exposed gate structure is the gate conductive layer 18.

Regarding claim 19, wherein the gate conductive layer comprises a polysilicon layer 18 and a metal silicide layer 20.

Regarding claim 20, the exposed gate structure is the metal silicide layer 20 and portions thereof are partially etched (fig. 3).

Regarding claim 21, a spacer 27 disposed on sidewalls of each gate structure, covering the line layer (thin pad oxide layer, see col 5, lines 25-30).

Regarding claim 22, wherein the lining layer is a rapid thermal oxide (RTO) layer (thin pad oxide layer, see col 5, lines 25-30).

Regarding claim 23, a spacer 27 covering the lining layer and material of the spacer is silicon nitride.

Set of claims 35- 42.

Claims 35- 42 are rejected under 35 USC 102 (b) as being anticipated by Chen et al. (6239011).

Chen et al. disclose a semiconductor structure with a partially etched gate, comprising:

a semiconductor substrate 10; a gate dielectric layer 16, a gate conductive layer 18-20 and a cap layer 1624, sequentially stacked on the substrate to form a gate structure; and

a lining layer (thin pad oxide layer, see col 5, lines 25-30) disposed on sidewalls of the gate structure, wherein the lining layer disposed on two sidewalls of the gate structure is partially etched to expose the adjacent gate structure 34 (col 2, line 30) (fig. 3).

Regarding claim 36, an inter-layer dielectric layer 26/28 covering the gate structure; and a contact formed in the inter-layer dielectric layer, exposing the substrate 10 and a portion of the gate structure 34 (col 2, line 30) therein, wherein the lining layer of the exposed portion of the gate structure is partially removed.

Regarding claim 37, the exposed gate structure is the gate conductive layer 18/20 (fig. 18A).

Regarding claim 38, wherein the gate conductive layer comprises a polysilicon layer 18 and a silicide layer 20.

Regarding claim 20, the exposed gate structure is the metal silicide layer 20 and portions thereof are partially etched (fig. 3).

Regarding claim 40, a spacer 27 covering the lining layer (thin pad oxide layer, see col 5, lines 25-30) and material of the spacer is silicon nitride.

Regarding claim 41, wherein the lining layer is a rapid thermal oxide (RTO) layer (thin pad oxide layer, see col 5, lines 25-30).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818